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Performance Improvement of Voltage-mode Controlled Interleaved Buck Converters

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ABSTRACT

This paper presents the performance improvement of voltage-mode controlled interleaved synchronous buck converters. This is a voltage-mode controlled scheme, where the controllers do not need an external saw-tooth generator for PWM generation and the loop design is easier. The controller implementation requires only a single error amplifier and gives almost current mode control performance. The control scheme uses voltage feedback with two loops similar to current mode control: one for the slow outer loop and the other for the faster inner PWM control loop. To improve the performance of the converter system a coupled inductor is used. This coupled inductor reduces the magnetic size and also improves the converter's transient performance without increasing the steady-state current ripple. The effectiveness of the proposed control scheme is demonstrated through PSIM simulations.

Keywords: Interleaved buck converter, Coupled inductor, Voltage-mode control, V^2 control, Ripple cancellation.

1. Introduction

In recent years the demand for dc-dc converters is increasing. Particularly, more attention is being focused on the development of compact power supplies that are lightweight and highly efficient with faster dynamics. DC-DC converters are widely used in switch-mode power supplies. To meet increased demands several new topologies are being developed that operate at a high efficiency and are simple to control. During the past three decades, several aspects of dc-dc converters have been explored. These include modeling and analysis; improving both the steady state and dynamic converter performance etc. In particular, the control of high frequency dc-dc converters has attracted much research due to the inherent difficulties in achieving the desired characteristics such as stiff line and load regulation, and robustness despite uncertainties in the converter parameters [1-3].

Boost topologies are suitable for universal applications whenever load voltage requirements are higher than the input supply voltage. Buck topologies are finding wide applications whenever load voltage is less than the input source voltage. But it operates in a discontinuous input current mode and has a serious disadvantage of a large input current ripple amplitude and EMI. In applications requiring lower voltage transformation ratios, one has to adapt buck topologies inspite of their larger input current ripple and EMI.

Parallel converters with new control strategies are being developed to increase the power processing capability and to improve the reliability of the power electronic system. In particular, dc-dc power conversion

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employing interleaved buck converters (IBC)[4-5] has several advantages, such as (i) ripple cancellation in the waveforms to maximum extent, (ii) lower value of ripple amplitude and (iii) higher ripple frequency in the resulting input and output waveforms. Further, parallel connection of converters also reduces maintenance problems while increasing the reliability and fault tolerance etc. In general, the interleaving technique consists of phase shifting the control signals of several converter cells (N) in parallel that operate at the same switching frequency. Maximum benefits of interleaving can be achieved if a phase shift of $2\pi/N$ is used for the control signals. The interleaving structure increases the number of inductors compared to the conventional converter. One way to overcome these shortcomings is to use integrated magnetic components, which reduces the core number and complexity of the converters. Furthermore, the integrated magnetic approach for the interleaved converters reduces the steady-state current ripple, the conduction losses in the switching devices and the core losses if proper core structure is employed.

Synchronous buck regulators [6-9] are the best choice for powering the microprocessor loads, as they are simple and have low cost topologies. They yield incredibly high efficiency even at low voltage and high currents. However, when powering the microprocessor loads with a single synchronous buck regulator, one has to optimize the output inductor and filter capacitor components to achieve the desired transient and steady-state performance requirements. To yield the faster dynamic response the output inductor must be as low as possible. But the lower value inductance increases the output voltage ripple deteriorating the steady-state performance. To overcome some of these shortcomings, multi-channel interleaved synchronous buck regulators with coupled inductors are proposed [10]. These interleaved buck converters are widely used for low voltage and high current applications, particularly, in powering the microprocessor loads. The coupled inductor can solve the problem of contradictory inductance requirements: a low inductance for getting faster transient response and a high inductance to achieve low steady-state current ripple.

Several controlling methods, including voltage mode, current mode and hysteretic control, have been reported

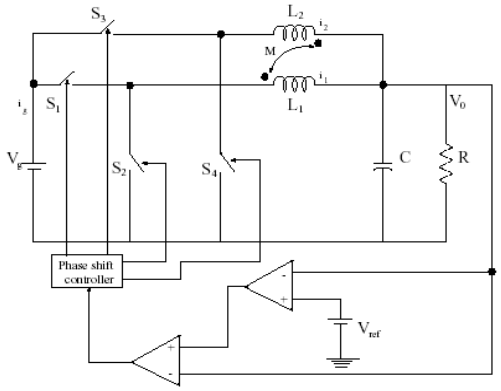

Fig. 1 2-cell interleaved buck converter with voltage-mode controller

for the dc-dc converters. Each of the above methods has their own advantages and disadvantages. However, the two-loop voltage mode V^2 control method is simple in its realization and achieves an almost similar response as that of current mode control. The main advantages of the V^2 control method are: (i) a simple controller with a low number of components, (ii) a compensation design that's quite easy, (iii) a dynamic response almost similar to the two-loop current mode control, (iv) the capability of compensating for any line or load variations because it allows a right duty ratio variation from 0 to 100%.

This paper explores the V^2 control of interleaved buck regulators and its performance improvement using an integrated magnetic structure. The effectiveness of the proposed voltage mode control is demonstrated against line and load variations. PSIM is used to implement the closed loop converter system. The paper is organized as follows. In Section 2 the principle of two-loop voltage-mode control is discussed. Large-signal response analysis and other simulation studies are discussed in Section 3. Conclusions follow in the final section of this paper.

2. The principle of two loop voltage-mode control

The V^2 control is a simple voltage mode type control as shown in Fig. 1. It uses two loops similar to the current mode control. However, this V^2 control is easy to implement by using an error amplifier, a compensator, and a PWM generator as shown in Fig. 2.

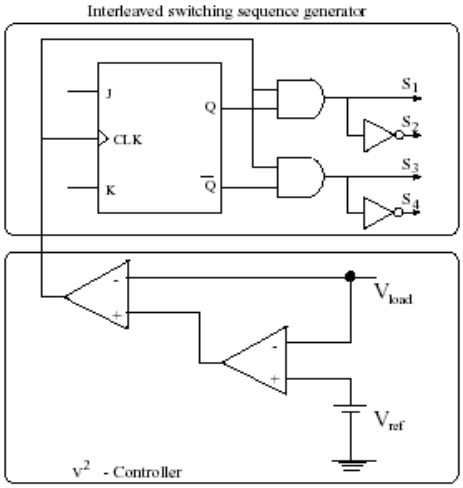

Fig. 2 Block diagram of a two-loop voltage-mode controller

The outer loop generates a control signal, depending on the error signal, to the PWM generator. The inner voltage loop comparator generates the PWM sequence to the switching devices. The controller in the outer loop, shown in Fig. 1 as simple Op-Amp, belongs to a class of compensators and will be designed depending on the converter stability requirements. Here a simple proportional plus integral controller is used. The load voltage is used as the PWM ramp signal and is fed to the PWM generator. Whenever there is a change in the supply it automatically reflects the slope of the load voltage. Since the load voltage is used as the PWM ramp, the corresponding duty ratio change, either increases or decreases, accordingly to maintain an almost constant load voltage. On the similar lines, changes in the load affect the load voltage. This in turn changes the pulse width of the PWM output to maintain the load regulation.

The PWM signal generated by the PWM comparator, depending on the control status, is used to generate the interleaved switching sequence. In the process of the interleaved switching sequence generating, from the single PWM pattern, a digital circuit consisting of J-K Flip-Flop and NOT gates is used as shown in Fig. 2. For the J-K Flip-Flop there is no need of providing an external clock and the PWM signal itself acts as a clock as well as one of the inputs of the logical AND, OR gates. Thus the switching sequence generator circuit is simple and its realization requires only three IC's, 7408N, 74LS04P, 74LS76AP.

3. Simulation Results and Discussions

The proposed V^2 controller based interleaved buck converter system is shown in Fig. 1. A simulator prototype converter system was implemented to study the regulation capability of the controller. The converter parameters are given in Table 1. In order to maintain the load voltage constant against the line and load disturbances, the converter duty ratio must be changed. This duty ratio is controlled by a PWM generator, obtained from the V^2 controller. The proposed V^2 controller based scheme is evaluated through PSIM simulations.

Table 1 Converter parameters

R_1	61 mΩ
R_2	108 mΩ
R	0.2 Ω
L_1	0.2 mH
L_2	0.2 mH
M	0.1 mH
C	10 μF
V_g	10 V

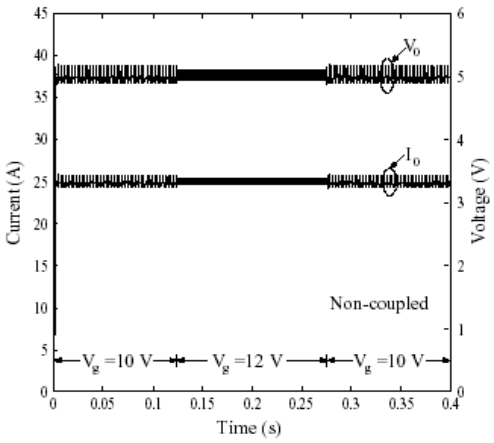

Fig. 3 V_0, I_0 response for supply disturbance (non-coupled)

Simulated load voltage regulation characteristics are presented for two cases: (i) a supply voltage change from 10 V to 12 V and (ii) a change of load resistance from 25 A to 30 A. For a given load, when the input line voltage changes from 10 V to 12 V the load voltage is almost constant and the variation is shown in Fig. 3, while Fig. 4

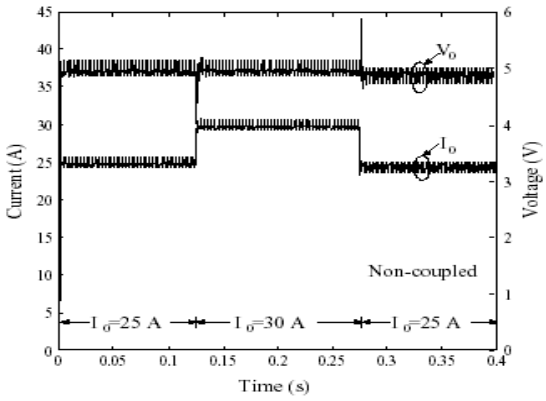

Fig. 4 V_0, I_0 response for load disturbance (non-coupled)

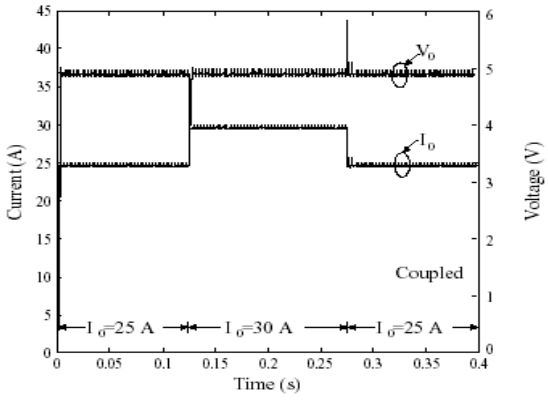

Fig. 6 V_0, I_0 response for load disturbance (coupled)

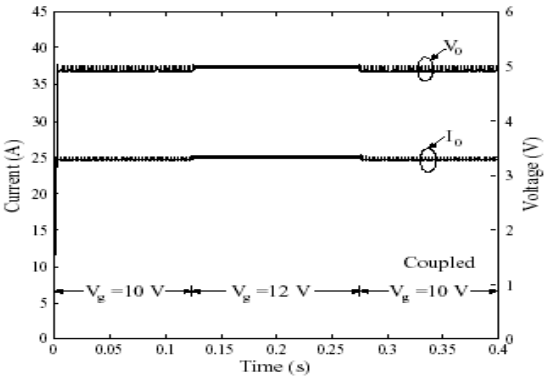

Fig. 5 V_0, I_0 response for supply disturbance (coupled)

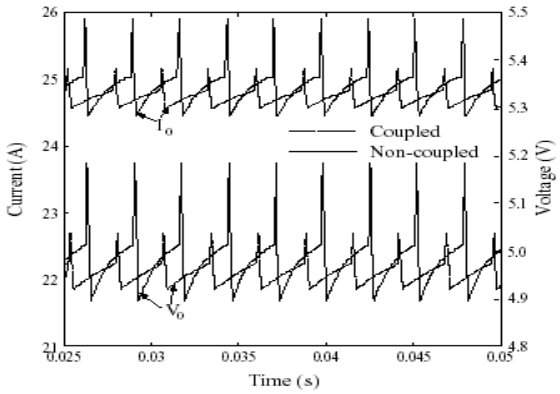

Fig. 7 Ripple magnitudes of V_0, I_0

indicates the load voltage regulation against the load disturbance. From the simulation results, it is observed that the two loop V^2 control strategy is a promising one with reference to the load voltage regulation under line and the load disturbances. However, there exists a substantial amount of ripple content both in the load voltage and current thus increasing the filtering requirement on the load side. In order to reduce this ripple content and to improve the steady-state performance without altering transient performance, a magnetic coupling is introduced among the two interleaved cells.

Studies were made to improve the steady-state performance of the V^2 controlled converter by incorporating the integrated inductance between two channels of the converter. This coupling inductance will not only give a compact magnetic design, but will also result in an improved converter performance. Simulation studies have been carried out for different values of coupling coefficients and nature of coupling. These simulation results indicate that among two possible coupling structures, direct and inverse coupling, the inverse coupling gives a better performance. This is because with inverse coupling the common-mode inductance is high. As a result the steady state current ripple is low and the corresponding power loss is also low. Furthermore, if the coupled inductor is designed such that $L_{nc}=(1+k)L_{cp}$, then the converter system exhibits the same transient response as that of a non-coupled case and reduces the steady-state current ripple. That means the integrated inductor is capable of giving two different inductance values, a lower value for transient conditions and a higher value for steady-state operating conditions. Where 'L_{nc}' - self-inductance of individual interleaved cells (non-coupled case), 'L_{cp}' and 'k' are the self-inductance and coupling coefficient of the integrated coupled inductor, respectively.

The dynamic responses of the converter system with coupling are given in Figs. 5 and 6. The transient responses are almost similar to that shown in Figs. 3 and 4. However, the steady-state ripple, both in the load voltage and current, is reduced. The enlarged load voltage and current waveforms both for coupled and non-coupled cases are given in Fig. 7. Ripple reduction is mainly present because of the coupling between the two channels. Although we may face difficulties in making an integrated inductor satisfying $L_{nc}=(1+k)L_{cp}$, it will improve the performance and reduce the space requirement of the power supply system. The performance of the V^2 controller is also verified for variable reference set point voltages and it is found that the controller is capable of adjusting the load voltage to the new reference voltages within a reasonable amount of time.

4. Conclusions

In this paper a two-loop voltage-mode control scheme for interleaved buck regulators was proposed. It has resulted in an almost exact performance as that of the current mode control but it does not require any current sensors. This is one of the main advantages of this scheme. The scheme was implemented in a PSIM environment where it demonstrated its performance. Further, an integrator inductor concept was used, which has improved the converter performance in addition to reducing its structure. Simulation studies have been presented taking coupling between the two interleaved channels into account. These studies reveal that the inverse coupling improves the steady-state performance of the converter without altering the dynamic response.

References

[1] Forsyth. A. J, Mollov. S. V, "Modeling and control of DC-DC converters," IEE Power Engineering Journal, Vol. 12(5), pp. 229 –236, 1998.

[2] R. B. Ridley, "A New continuous time model for current mode control," IEEE Trans. On Power Electronics, Vol. 6(2), pp. 271-280, 1991.

[3] Lautaro D. Salazar, Phoivos D. Ziogas, "A novel current assisted output voltage control technique for switch-mode rectifier converters," IEEE Trans. On Power Electronics, Vol. 7(3), pp. 444-452, 1992.

[4] Wi Gu, Issa Batarseh, "Interleaved synchronous buck regulator with hysteretic voltage control," Proc. of IEEE PESC'01, pp. 1512-1516, 2001.

[5] Jaber A. Abu-Qahouq, Jia Luo, Issa Batarseh, "Voltage regulator module with interleaved synchronous buck converters and novel voltage mode hysteretic control," Proc. of IEEE Midwest Symposium on Circuits and Systems (MWSCAS'2001), pp. 972-975, 2001.

[6] George Schuellein, "Current sharing of redundant synchronous buck regulators powering high performance microprocessors using the V^2 control," Proc. of IEEE APEC'98, pp. 853-859, 1998.

[7] Wenkang Huang, "A new control for multi-phase buck converter with fast transient response," Proc. of IEEE APEC'01, pp. 273-279, 2001.

[8] Song Qu, "Modeling and design considerations of V^2 controlled buck regulator." Proc. of IEEE APEC'01, pp. 507-513, 2001.

[9] Veerachary. M, "V^2 control of cascade buck converters," IEEE Telecommunications Energy Conference, INTELEC '2003, pp. 470 – 472, 2003.

[10] Pit-Leong, Peng Xu, Bo Yang, Fred. C. Lee, "Performance improvements of interleaving VRM's with coupling inductors," IEEE Trans on Power electronics, Vol. 16(4), pp. 499-507, 2001.

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